DEMODULATOR FOR DEMODULATING DIGITAL BROADCAST SIGNALS

TECHNICAL FIELD

The present invention relates to a digital broadcast demodulator for demodulating a digital modulated signal modulated, for example, by multi-value VSB modulation, in digital broadcast for digital transmission by coding video and audio information.

BACKGROUND ART

Recently, owing to the advancement in the digital compression technology and digital modulation and demodulation technology, the television broadcast is presented by using satellites and CATV. The video data is coded by MPEG2, and the digital modulation system is realized by the QPSK method in satellite broadcast or QAM method in CATV. In the United States, the terrestrial digital broadcast (DTV) is scheduled from the fall of 1998, and the digital modulation 8VSB system by video compression by MPEG2 is planned.

Referring to the drawing, a conventional example of receiving and demodulating apparatus of digital terrestrial broadcast is explained below.

Fig. 10 is a block diagram of a demodulator of terrestrial digital broadcast. An RF modulated wave signal received by an antenna 1 which receives an RF signal is put into a tuner 2 which selects a channel, and an arbitrary channel is selected. In the tuner 2, the selected signal is controlled of gain, and converted in frequency, and is issued as an intermediate frequency (IF). The IF output from the tuner 2 is limited in band in the frequency characteristic determined in a SAW filter 3, and is put into an amplifier 4 which amplifies a signal.

In the amplifier4, by a control signal from an AGC detector 11

explained later, the signal level is controlled, and is supplied into mixers 5, 6. In the mixers 5, 6, the IF signal is multiplied by the local frequency signal from a voltage control oscillator 8 (VCO) to undergo quadrature detection. After quadrature detection, base band signals of I, Q signals are supplied into LPF 9 and LPF 10, individually.

Herein, the mixer 6 delivers a beat signal generated by the difference between the IF carrier frequency and the frequency signal from the VCO 8, and it is put into the LPF 9, and is supplied into the VCO 8 as frequency error signal. A reproduction carrier from the VCO 8 is put into the mixer 5, and a carrier delayed in phase by 90 degrees is supplied into the mixer 6 through a 90-degree phase shifter 7 for delaying the phase by 90 degrees. By constituting a PLL by the system of the mixer 6, LPF 9, VCO 8 and 90-degree phase shifter 7, the local signal equal to the IF carrier frequency of the reception modulated wave can be oscillated by the VCO 8.

The base band signal supplied into the LPF 10 is limited to a desired frequency characteristic, and is supplied into an A/D converter 12 for converting an analog signal into a digital signal, and the AGC detector 11 for determining the average of signal amplitude. In the AGC detector 11, detecting the envelope of the entered base band signal, an AGC control signal is generated. As the AGC control signal is fed back to the amplifier 4 and tuner 2 and controlled, the AGC operation is carried out.

On the other hand, the base band signal supplied into the A/D converter 12 is converted into a digital signal, and is supplied into a demodulation processing unit and a waveform equalizer 12 in a later stage. The digital data delivered from the A/D converter 12 is put into a BPF 13, and a half frequency component of the symbol frequency (Fs) of data speed is extracted.

Being supplied into a square circuit 14, the frequency component of Fs/2 is squared, and is put into a BPF 15. In the BPF 15, a frequency

component Fs equal to the symbol speed is extracted, and put into a phase detector 16 which detects a phase error. In the phase detector 16, a phase error from the symbol frequency (Fs) is detected, and supplied into a loop filter 17.

In the loop filter 17, the phase error signal is integrated, and supplied as control signal of VCO 18. By constituting the feedback loop to the BPF (Fs/2) 13, square circuit 14, BPF (Fs) 15, phase comparator 16, loop filter 17, and VCO 18, the clock is regenerated.

Further, the output digital data from the A/D converter 12 is supplied into a symbol judging circuit 19 for judging the value of the symbol data, and the value of the received symbol data is judged, and supplied into a synchronous signal detecting circuit 21 for detecting the synchronous signal in the reception data. In the synchronous signal detecting circuit 21, comparing with the symbol data value of the synchronous reference signal from a known data circuit 20 of synchronous signal for delivering the data value of known synchronous signal, the synchronous signal of packet data is detected.

Thus, in order to demodulate the digital terrestrial broadcast 8VSB or the like, important steps are synchronous signal detection processing of transmission packet data, AGC processing for controlling signal amplitude, and clock regeneration for extracting and regenerating clock component from transmission data.

However, in the event of occurrence of inferior environments for receiving broadcast, such as characteristic ghost and multipath of digital terrestrial broadcast, and same channel interference by NTSC or other analog broadcast, it is extremely difficult to detect the synchronism, operate the AGC or regenerated the clock precisely in such synchronous detection processing by precisely judging the data value of the symbol, AGC processing by determining the average of detected base band signals, or clock regeneration processing of extracting the frequency components in the transmission data. Accordingly, in order

to raise the precision, it was required to process by heightening the sampling frequency, or compose the filter by a considerably large circuit.

SUMMARY OF THE INVENTION

To solve the above problems, the digital broadcast demodulator of the invention is characterized by, in one aspect, comprising a circuit for establishing the synchronous signal in reception data by processing only the most significant bit (MSB) showing the positive or negative sign of the reception transport packet data.

In such constitution of the invention, even in an inferior radio wave condition of strong ghost or multipath interference characteristic of digital terrestrial broadcast, the synchronous signal in the packet can be detected and established stably by an extremely inexpensive circuit constitution.

It is a second aspect of the digital broadcast demodulator of the invention to regenerate the clock by phase control on the basis of a phase error, by determining the difference of synchronous signals of the reception packet data which should be originally at the same level, and detecting the clock phase error of transmission data.

In this constitution of the invention, by detecting the phase error of clock of reception data and feeding back to the VCO for controlling, even in an inferior radio wave condition of strong ghost, multipath interference or low C/N characteristic of digital terrestrial broadcast, the clock can be regenerated stably and precisely by an extremely inexpensive circuit constitution.

A third aspect of the digital broadcast demodulator of the invention is characterized by detecting the synchronous signal in the received packet data, determining the difference between the data value of the detected synchronous signal and the reference value, and controlling the AGC on the basis of this difference.

In this constitution of the invention, a precise AGC is realized even in an inferior radio wave condition.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a general block diagram of a digital broadcast demodulator of the invention, Fig. 2 is an essential block diagram of digital broadcast demodulator in a first embodiment of the invention, Fig. 3 is an essential block diagram of digital broadcast demodulator in a second embodiment of the invention, Fig. 4 is an essential block diagram of digital broadcast demodulator in a third embodiment of the invention, Fig. 5 is a data frame diagram of digital terrestrial broadcast VSB modulation system, Fig. 6 is a field synchronous signal diagram of digital terrestrial broadcast VSB modulation system, Fig. 7 is a sample waveform diagram of segment synchronous signal explaining the second embodiment of the invention, Fig. 8 is a waveform diagram of segment synchronous signal explaining the third embodiment of the invention, Fig. 9 is a block diagram of clock phase error detecting circuit of the invention, and Fig. 10 is a block diagram showing a constitution of a digital broadcast demodulator in a prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, preferred embodiments of the invention are described below. First in Fig. 1, the digital broadcast demodulator of the invention is described, particularly about the schematic constitution of the digital broadcast demodulator of digital terrestrial broadcast VSB modulation system, and then the embodiments corresponding to the claims of the invention are specifically described.

The parts having the same functions as in Fig. 10 showing a conventional reception demodulator of digital terrestrial broadcast are identified with same reference numerals, and detailed description is omitted.

Output digital data, Data, of an A/D converter 12 is divided into four portions. One of them is put into a synchronous (sync) code pattern detecting circuit 101 of a segment synchronism detection establishing circuit block 116, and synchronous pattern is detected by processing the code bit (most significant bit, MSB, showing positive or negative sign). The output of the synchronous code pattern detecting circuit 101 is divided into three portions, which are individually supplied into a detection protection counter circuit 103, a segment synchronism detection establishing circuit 104, and a clock phase error detecting circuit 105.

The output of the segment synchronism detection establishing circuit 104 for judging the true synchronous pattern of each segment is supplied into a symbol number counter 102 as a reset signal, and the counting result of the number of symbols in one packet is fed back into the detection protection counter 103 and segment synchronism detection establishing circuit 104. The detection protection counter 103 sends out a segment start signal Segst showing the position of the segment synchronous signal in the packet on the basis of the fed-back information to a terminal 109, and a segment synchronism establishment signal Shld showing the detection establishment of the segment synchronous signal to a terminal 110.

The segment synchronism establishment signal Shld is put into a switch circuit 111 to become a switch signal for changing over a control signal Gerr from an AGC error detecting circuit 106 mentioned below and a control signal from the AGC detector circuit 11.

The second output digital data, Data, branched from the A/D converter 12 is supplied into the clock phase error detecting circuit 105, and is fed together with the signal from the synchronous code pattern detecting circuit 101 and the segment start signal Segst from the detection protection counter 103, and a clock phase error of data is issued as clock regeneration control signal Pherr to the terminal 108.

This clock regeneration control signal Pherr is put into a D/A converter 112, and is converted into an analog signal, which is fed into the LPF 113. The control signal integrated in the LPF 113 is put into the VCO 18 to control its oscillation frequency. A feedback loop is composed in the flow of the VCO 18, A/D converter 12, clock phase error detecting circuit 105, D/A converter 112, and LPF 113.

Further, the third divided output of digital data, Data, of the A/D converter 12 is put also into the AGC error detecting circuit 106, and issued into the terminal 107 as an AGC control signal Gerr as the different from the known value. This AGC control signal Gerr is put into the D/A converter 114, and is converted into an analog signal, and is supplied into the LPF 115. The AGC control signal integrated in the LPF 115 is supplied into the switch circuit 111.

The switch circuit 111 changes over, by the segment establishment signal Shld, between the control signal from the analog AGC detector 11 and the AGC control signal from the LPF 115 detected by digital processing. The AGC control signal as output from the switch circuit 111 is put into the amplifier 4 and tuner 2, and the amplitude of the input signal is controlled.

The fourth output of the A/D converter 12 is put into the waveform equalizer 22 to be a reception output.

In thus constituted digital broadcast demodulator, specific embodiments corresponding to the claims are described below.

(Embodiment 1)

Fig. 2 shows an essential block diagram of the embodiment corresponding to claims 1, 2, 3 of the invention. This embodiment relates to a digital broadcast demodulator used in an apparatus for receiving digital broadcast by transmitting coded digital video and digital audio information in packet form, in which, particularly in digital VSB transmission system, the circuit is constituted to process the code bit (MSB) of reception transport packet data, and the

synchronous signal in the reception data is established. In this constitution, even in an inferior radio wave condition for receiving broadcast, such as ghost, multipath, or same channel interference of NTSC, the synchronous signal in the packet can be detected and established precisely and securely.

Referring now to Fig. 2, the constitution and operation are described below. In the demodulator of the invention, the base band signal after quadrature detection is put into the A/D converter 12, and the clock regeneration has been already locked. Of the output digital data, Data, from the A/D converter 12, the code bit (MSB) is supplied into the synchronous code pattern detecting circuit 101 and symbol number counter 102 in the segment synchronism detection establishing circuit block 116. Herein, the data structure of packet of VSB digital terrestrial broadcast is shown in Fig. 5 and Fig. 6. The transmission frame shown in Fig. 5 is composed of 832 symbols in one packet, and the segment synchronous signal is inserted by the portion of four symbols only from the beginning.

In every 313 packets (segment), field synchronous signals #1, #2 are inserted. Fig. 6 shows the field synchronous signal. At the beginning of the packet, a segment synchronous signal of four symbols, and a specific number of PN codes are composed. The segment synchronous signal is a mapping signal in the values of +5, -5, -5, +5 as shown in Fig. 6. This signal value is the known data, and is inserted at the beginning of all packets as shown in Fig. 5.

In the synchronous code pattern detecting circuit 101, the code bit (MSB) of all reception data is processed, and +, -, -, + as code pattern of segment synchronous signal are detected. When processing the signal by the complement of 2, the codes of the segment synchronous signal are -, +, +, -.

When processing the code bits only, even in the presence of strong ghost, multipath interference or NTSC same channel interference

characteristic of digital terrestrial broadcast, the reception data receives considerably effects of impedance, and deterioration occurs. However, the code bit information is extremely strong against effects of interference even in the inferior reception wave situation, so that the synchronous pattern of the segment synchronous signal can be detected stably.

When detecting the synchronous pattern for four symbols in all reception data in the synchronous code pattern detecting circuit 101, simultaneously, signal Sdet is issued to the detection protection counter 103 and segment synchronous detection establishing circuit 104. In the symbol number counter 102, when the power is supplied, power-on reset is applied and synchronized with the signal processing clock equal to the symbol speed Fs, thereby starting automatic count-up. When counting 832 symbols in one packet, a count-up signal Co is issued to the detection protection counter 103 and segment synchronism detection establishing circuit 104.

In the segment synchronism detection establishing circuit 104, synchronous pattern detection signal Sdet, symbol number count-up signal Co, and signal Shld from detection protection counter 103 are supplied, if there is same pattern as the segment synchronous code pattern in all reception data, it is judged which pattern is the true segment synchronous signal.

In the operation of the segment synchronism detection establishing circuit 104, when either the signal Co issued when the symbol number counter 102 reaches the symbol number count 832 of the packet, or the segment synchronous code pattern detection signal Sdet from the synchronous code pattern detecting circuit 101 is entered, an output signal Lo is issued.

Usually, in the reception data, there are many code pattern data same as the segment synchronous code pattern, but the symbol number counter 102 is once reset when the same code pattern detection signal

Sdet as the segment synchronous signal is fed into the segment synchronism detection establishing circuit 104, and Lo signal for dropping to Low by the portion of one clock is entered, and counts up to 832 which is the number of symbols in one packet. In the midst of counting up, when the same pattern as the synchronous code pattern is detected, the segment synchronism detection establishing circuit 104 issues signal Lo and resets the symbol number counter 102. Thus, the counting operation is repeated until the signal Sdet is entered simultaneously with the output of signal Co of count-up of symbol number 832 of one packet. That is, in the case of a true segment synchronous signal, when counting of 832 is over, simultaneously, there is a segment synchronous signal of next packet, and the signal Sdet and signal Co are simultaneously entered into the segment synchronism detection establishing circuit 104, and Lo signal is issued, and the symbol number counter 102 is reset.

The output signal Co of the symbol number counter 102 and the output signal Sdet of the synchronous pattern detecting circuit 101 are also supplied into the detection protection counter 103. As a result, the detection protection counter 103 sets high the hold signal Shld once every time, and by this signal Shld, the segment synchronism detection establishing circuit 104 is held, and it is held in the state that the reset signal Lo is not issued until the signal Sdet from the circuit 101 and signal Co from the circuit 102 are entered simultaneously. Therefore, if only Sdet signal is entered in the meantime, the reset signal Lo is not issued. At this first time, however, if signal Co is next entered in the circuit 103, unless the signal Sdet is entered at the same time, the symbol number counter 102 and detection protection counter 103 are reset, and the signal Shld is low. In the detection protection counter 103, counting the number of times of simultaneously input of signal Sdet and signal Co, and when Sdet and Co are entered simultaneously by the specified number of times, for example, four times

consecutively, it is detected and established as the true segment synchronous signal in the reception data. The reason is that, in the case of output of signal Co, it is possible that signal of same pattern, but not the true segment synchronous signal may entered by accident, and such possibility is avoided. Thus, when the segment synchronous signal in the reception data is detected and established repeatedly by a specified number of times, the segment establishment signal Shld is fixed at high level.

By this Shld signal, the segment synchronism detection establishing circuit 104 is held, and it is held in the state that the reset signal Lo is not issued until the Sdet signal from the circuit 101 and Co signal from the circuit 102 are entered at the same time. Therefore, if only Sdet signal is entered in the meantime, the reset signal Lo is not issued. Even in this hold state, only when the signal Sdet and signal Co are entered simultaneously, reset signal Lo is issued, and the symbol number counter 102 is updated.

Once the segment synchronous signal is established, if signal Sdet and signal Co are not entered simultaneously, the segment establishment is not canceled immediately, but when making mistakes by a specified number of times, for example, eight times or more, the establishment of segment synchronous signal detection is canceled, and the signal Shld is set to low level.

Thus, while resetting the symbol number counter 102 every time the same waveform as the segment synchronous signal is detected, when reset by a true segment synchronous signal and similar waveform to the synchronous signal is not entered until counting up the specified number, count-up of the symbol number counter 102 and incoming of true synchronous signal of next segment occur simultaneously, and signal Shld is issued from the detection protection counter, and similar waveform while counting up the circuit 102 is eliminated, and when this operation is repeated by a specified number of times, it is detected and established

as true segment synchronous signal.

The constitution of this embodiment comprises the synchronous code pattern detecting circuit 101 for detecting the known synchronous signal code pattern by processing only the code bit (MSB) of the reception data, symbol number counter 102 for counting the number of symbols in one packet, segment synchronism detection establishing circuit 104 for judging true segment synchronous code pattern when the symbol number counter 102 detects the specified count while detecting the synchronous signal code pattern at the same time, and issuing a signal for resetting the symbol number counter 102, and detection protection counter circuit 103 for issuing signal Shld by detecting and establishing the segment synchronous signal in the reception data from the output of the synchronous code pattern detecting circuit 101 and the count-up of specified number of the symbol number counter circuit 102, and therefore even in an inferior radio wave condition for receiving broadcast such as strong ghost or multipath characteristic of digital broadcast, same channel interference of NTSC broadcast, low C/N, and others, the synchronous signal can be detected and established stably, and decoding can be processed stably.

(Embodiment 2)

Fig. 3 shows a block diagram of embodiment 2 corresponding to claims 4, 5, 6, 7 of the invention. This embodiment relates to a digital broadcast demodulator used in an apparatus for receiving digital broadcast by transmitting coded digital video and audio information in packet form, in which, particularly in digital VSB transmission system, the clock phase error of reception data is obtained by calculating the difference of N-th and N+1-th (N > 1) packet synchronous signals of reception data, and the clock is regenerated stably even in an inferior radio wave reception circumstance.

Referring now to Fig. 3, the constitution and operation are described below. The broken line block 116 corresponds to the segment

synchronism detection establishing circuit block shown in Fig. 2 of embodiment 1, and it issues the segment synchronism establishing signal Shld showing establishment of detection of segment synchronous signal in the reception data, Data, and segment start signal Segst showing the position of the segment synchronous signal in the packet. The operation of block 116 is same as explained in embodiment 1, and is omitted.

The reception digital data output, Data, from an A/D converter 12 is put into a clock phase error detecting circuit 105. The segment synchronism detection establishing circuit block 116 also feeds the signal Sdet showing the position of the same data as the code pattern of the synchronous signal in the packet data and the signal Segst showing the position of segment signal in the packet data.

Fig. 9 shows a block diagram of clock phase error detecting circuit 105. The digital data, Data, from the A/D converter 12 is put into an addition input of an subtracting circuit 202 through a latch 203. This input is further put into a subtraction input of the subtracting circuit 202 through a latch 204. In the subtracting circuit 202, the N-th input is subtracted from the N+1-th input, and the subtraction value is put into a latch circuit 207. The sequence of subtraction operations is not limited, but it is important whether the value becomes 0 or not. In the latch circuit 207, the data is latched by the signal Sdet of code pattern detection of segment synchronous signal, and issued into a latch circuit 208. The signal Sdet is adjusted in time so as to latch the subtraction value at the timing after subtraction operation of the second and third segment synchronous signals of reception data by the latch circuit 205. In the latch circuit 208, by latching by the signal Segst showing the position of the segment synchronous signal to be sent out after detecting and establishing the segment synchronous signal, it is sent out as clock phase error signal Pherr. The signal Segst is also adjusted in time to the timing to be latched by the latch circuit 208, by the subtracted values of the second and third segment synchronous

signals in the latch circuit 206.

This circuit is constituted so as to detect segment synchronous signals of four symbols as shown in Fig. 7, and if using a different code pattern, the circuit may be composed differently.

Fig. 7 shows sample points of thus obtained segment synchronous signal unit. The sample points are a, b, c, d when the oscillation frequency of the VCO 18 is completely matched in phase with the clock of the reception data. The data values are smooth values because the band is limited so as not to cause inter-code interference by filtering processing of the SAW filter 3 in the preceding stage. Herein, supposing the N-th data to be the second data value b, by subtraction from the N+1-th data value c, c-b is processed.

As shown in Fig. 7, the subtraction processing is to determine the inclination of the linking line of sample point values b and c, or b' and c', which should be originally of the same level. Herein, when the clock of the reception data and the phase of the frequency signal oscillated by the VCO 18 are synchronized completely, the value of c-b is 0. If the frequency or phase is deviated, as indicated by broken line in Fig. 7, it is like c'-b', and the clock phase error signal Pherr is determined by subtraction process. Feedback control is executed so that this clock phase error signal Pherr may be close to 0. As shown in Fig. 1, the clock phase error is fed into the D/A converter 112 to be converted into an analog signal, and is supplied into the LPF 113. The clock phase error converted into analog signal is integrated in the LPF 113, and is supplied into the VCO 18 as clock phase control signal. In the VCO 18, the oscillation frequency signal is controlled on the basis of the clock phase control signal, and it is synchronized with the clock signal of the reception data by the PLL. In this example, the level is compared between two consecutive signals which should be originally of the same level, but if not consecutive, the level may be compared between two signals which are supposed to be of the same level

by nature.

Incidentally, according the invention as set forth in claim 7, when turning on the power or changing over the channels, until the segment synchronous signal of the packet is detected and established, it is intended to finish the clock regeneration quickly by feeding back the differential value of all data that should be originally of the same level matched between the synchronous signal and code pattern in the packet data, continuously to the VCO 18 as clock phase error.

In this embodiment, from the signal Segst showing the position of the synchronous signal of the data being sent out in packet form and the signal Sdet showing the synchronous signal in the packet data and the code pattern are the same data, the N-th and N+1-th synchronous signals of the packet data which are originally of the same level are processed by subtraction, and the clock phase error signal Pherr is determined, and the clock regeneration process is executed to control so that the error may be 0.

In this constitution, even in an inferior radio wave condition for receiving digital broadcast, the clock regeneration is realized stably in a very simple and inexpensive circuit constitution.

(Embodiment 3)

Fig. 4 shows a block diagram of embodiment 3 corresponding to claims 8, 9, 10 of the invention. This embodiment presents a digital broadcast demodulator, that is, a digital broadcast demodulator for receiving digital broadcast by transmitting coded digital video and audio information in packet form, in which, particularly in digital VSB transmission system, the synchronous signal is detected in the received packet data, and from the synchronism detection establishment signal and the signal showing the position of the synchronous signal in the packet, the difference between the data value of synchronous signal and the reference value is calculated, and thereby AGC is realized.

Referring now to Fig. 4, the constitution and operation are

described below. The broken line block 116 corresponds to the segment synchronism detection establishing circuit block shown in embodiment 1, and it issues the segment synchronism establishing signal Shld showing establishment of detection of segment synchronous signal in the reception data, Data, and segment start signal Segst showing the position of the segment synchronous signal in the packet. The operation of block 116 is same as explained in embodiment 1, and is omitted. The digital data output, Data, from an A/D converter 12 is put into an AGC error detecting circuit 106.

Fig. 8 shows segment synchronous signals of four symbols added to the beginning of packet data. The segment synchronous signal is mapped in the values of ±5 as shown in Fig. 8. Since these are known values, at the reception side, the data values corresponding to ±5 may be possessed as reference values. When the segment synchronism establishing signal Shld is entered in the AGC error detecting circuit 106, from the signal Segst showing the position of the segment synchronous signal in the packet, the position of the data of four symbols from the beginning of the segment synchronism is specified, and the difference of this value and the internal reference value is determined. As shown in Fig. 8, when the reception data is entered as indicated by broken line, the difference from the reference value is as indicated by d at the + side, and d' at the - side. Feedback control is executed so that the differences d, d' from the reference value may be closer to 0.

This is to show a case in which reception data larger than the reference value of segment synchronous signal is entered, but when data smaller than the reference value is entered, by subtracting after absolute value processing so that the code may not be inverted by subtraction process to increase the differential value, the error signal Gerr is issued as AGC control signal. The AGC control signal Gerr is put into the D/A converter 114 from the terminal 107 as shown in Fig.

1, and is converted into an analog signal and is supplied into the LPF 115. The AGC control signal integrated by the LPF 115 is fed into the amplifier 4 and tuner 2 through the switch circuit 111, and by feedback control, the amplitude of the reception data is controlled to realize AGC.

According to claim 10 of the invention, when turning on the power or changing over the channels, until the segment synchronous signal in the packet data is detected and established, it is intended to change over the AGC control signal between the control signal of detecting the amplitude error from the envelope of the analog signal and the control signal of detecting the amplitude error from the synchronous level by digital processing, by supplying the segment synchronism establishing signal Shld issued from the terminal 110 shown in Fig. 1 into the switch circuit 111. When the reception data is entered, until the segment synchronous signal of the packet is detected and established, the amplitude error is detected from the envelope of the base band signal by analog detection in the analog processing unit in the preceding stage, and the AGC control on the basis of this error is applied by priority, and after detecting and establishing the segment synchronous signal in the packet, the error signal from digital processing for detecting the amplitude error from the synchronous signal is fed back, and the AGC is done efficiently.

In this embodiment 3, from the signal Segst showing the position of synchronous signal of data sent in packet form, and the signal Shld showing the detection and establishment of the synchronous signal, by subtraction processing of the segment synchronous signal of reception data and reference value of segment signal, the amplitude error signal Gerr is determined, and D/A converted, and integrated by LPF, and fed back to the analog amplifier and tuner through the switch circuit 111, there by controlling the amplitude and realizing AGC. In this method, even in an inferior radio wave condition for receiving digital broadcast,

such as ghost and multipath, the AGC is realized stably in a very inexpensive circuit constitution.

In the foregoing embodiments, the demodulator of terrestrial digital broadcast is shown, but it may be also applied in other applications.

The number of symbols, the number of segments, the constitution of pulses of parts, and detail of signal format may be changed or modified within the scope of the claims.

Of course, the operation of individual circuits in the embodiments may be also realized by processing of microprocessor.

INDUSTRIAL APPLICABILITY

As described herein, the digital broadcast demodulator of the invention, relating to digital terrestrial broadcast of packet data or the like, comprises a synchronous pattern detecting circuit for processing code bits of reception data and detecting synchronous signal pattern, a symbol number counter circuit, a synchronism detection protection counter circuit, and a synchronism detection establishing circuit, in which the true synchronous signal pattern is established and detected, and therefore even in an inferior radio wave condition, such as strong ghost and multipath interference characteristic of digital terrestrial broadcast, the synchronous signal in the packet can be established and detected stably in a very inexpensive circuit constitution.

Also comprising subtracting means of reception data, by determining the level difference between synchronous signals which should be of the same level by nature, from the same code pattern detection signal as the synchronous signal and the signal showing the position of synchronous signal in the packet, the clock phase error of reception data is detected, and fed back to the VCO for controlling, and therefore even in an inferior radio wave condition, such as strong ghost and

multipath interference characteristic of digital terrestrial broadcast, low C/N, and others, the clock can be regenerated stably and precisely in a very inexpensive circuit constitution.

Further, by subtracting the synchronous signal of reception data and known reference value from the signal showing the position of synchronous signal in the reception packet data and the signal detecting and establishing the synchronous signal in the packet data, the amplitude error is determined, and fed back to the analog amplifier circuit and tuner for controlling, so that precise AGC is realized even in an inferior radio wave environment.